UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/625,904	07/24/2003	Ritsuko Kawasaki	0756-7181	1203

31780 7590 02/26/2008

ERIC ROBINSON
PMB 955
21010 SOUTHBANK ST.
POTOMAC FALLS, VA 20165

EXAMINER	
SEFER, AHMED N	

ART UNIT	PAPER NUMBER
2826	

MAIL DATE	DELIVERY MODE
02/26/2008	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/625,904	KAWASAKI ET AL.	
	Examiner	Art Unit	
	Ahmed Sefer	2826	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *19 November 2007*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-4 and 11-22* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-4 and 11-22* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *11/19/2007*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Response to Amendment

1. The amendment filed November 19, 2007 has been entered; no new claims have been introduced.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

3. Claims 1, 3 and 15 are rejected under 35 U.S.C. 102(e) as being anticipated by Adachi.

Adachi discloses in fig. 1 a semiconductor device comprising: a light-transmitting substrate 31; a base film 34 having a projection, the film being formed over one surface of the light-transmitting substrate; and an island-like semiconductor layer 35 having a crystal structure entirely covering the projection and extending over a pair of edges of the projection, a gate insulating film 51 over the island-like semiconductor layer; and a gate electrode 52 over the gate insulating film.

Note that during patent examination, the pending claims must be given their "broadest reasonable interpretation consistent with the specification." In re Hyatt, 21 1 F.3d 1367, 1372, 54 USPQ2d 1664, 1667 (Fed. Cir. 2000). While the claims of issued patents are interpreted in

light of the specification, prosecution history, prior art and other claims, this is not the mode of claim interpretation to be applied during examination. During examination, the claims must be interpreted as broadly as their terms reasonably allow. In re American Academy of Science Tech Center, WL 1067528 (Fed. Cir. May 13, 2004) (The USPTO uses a different standard for construing claims than that used by district courts; during examination the USPTO must give claims their broadest reasonable interpretation). This means that the words of the claim must be given their plain meaning unless applicant has provided a clear definition in the specification. In re Zletz, 893 F.2d 319, 321, 13 USPQ2d 1320, 1322 (Fed. Cir. 1989); Chef America, Inc. v. Lamb-Weston, Inc., 358 F.3d 1371, 1372, 69 USPQ2d 1857 (Fed. Cir. 2004). In the instant case the claim language "projection" is interpreted to mean "an extension beyond the normal line or surface." Therefore, it is clear that Adachi shows the semiconductor layer entirely covering the projection.

Re claim 3, the specification contains no disclosure of either the critical nature of the claimed arrangement or any unexpected results arising therefrom. Where patentability is said to be based upon particular chosen dimensions or upon another variable recited in a claim, the applicant must show that the chosen dimensions are critical. In re Woodruff, 919 F.2d 1575, 1578, 16 USPQ2d 1934, 1936 (Fed. Cir. 1990).

Re claim 15, Adachi discloses (col. 5, lines 62-63) a silicon oxide base film or silicon nitride base film.

4. Claims 2, 4 and 16 are rejected under 35 U.S.C. 102(e) as being anticipated by Adachi.

Adachi discloses in fig. 1 a semiconductor device comprising: a light-transmitting substrate 31; a base film 34 having a projection, the film being formed over one surface of the

light-transmitting substrate; a thin film transistor comprising an island-like semiconductor layer 35 comprising a channel formation region (unnumbered), wherein at least a part of the channel formation region being provided over the projection and wherein the island-like semiconductor layer entirely covers the projection and extends over a pair of edges of the projection; and a gate insulating film 51 over an island-like layer; and a gate electrode 52 over the gate insulating film.

Note that during patent examination, the pending claims must be given their "broadest reasonable interpretation consistent with the specification." In re Hyatt, 21 1 F.3d 1367, 1372, 54 USPQ2d 1664, 1667 (Fed. Cir. 2000). While the claims of issued patents are interpreted in light of the specification, prosecution history, prior art and other claims, this is not the mode of claim interpretation to be applied during examination. During examination, the claims must be interpreted as broadly as their terms reasonably allow. In re American Academy of Science Tech Center, WL 1067528 (Fed. Cir. May 13, 2004) (The USPTO uses a different standard for construing claims than that used by district courts; during examination the USPTO must give claims their broadest reasonable interpretation). This means that the words of the claim must be given their plain meaning unless applicant has provided a clear definition in the specification. In re Zletz, 893 F.2d 319, 321, 13 USPQ2d 1320, 1322 (Fed. Cir. 1989); Chef America, Inc. v. Lamb-Weston, Inc., 358 F.3d 1371, 1372, 69 USPQ2d 1857 (Fed. Cir. 2004). In the instant case the claim language "projection" is interpreted to mean "an extension beyond the normal line or surface." Therefore, it is clear that Adachi shows the semiconductor layer entirely covering the projection.

Re claim 4, the specification contains no disclosure of either the critical nature of the

claimed arrangement or any unexpected results arising therefrom. Where patentability is said to be based upon particular chosen dimensions or upon another variable recited in a claim, the applicant must show that the chosen dimensions are critical. In re Woodruff, 919 F.2d 1575, 1578, 16 USPQ2d 1934, 1936 (Fed. Cir. 1990).

Re claim 16, Adachi discloses (col. 5, lines 62-63) a silicon oxide base film or silicon nitride base film.

5. Claims 11 and 13 are rejected under 35 U.S.C. 103(e) as being unpatentable over Adachi.

Adachi discloses in fig. 1 a semiconductor device comprising a light-transmitting substrate 31, a base film 33 having a region of a first thickness and a region of a second thickness over one surface of the light- transmitting substrate, wherein the second thickness is smaller than the first thickness (fig. 3 and col. 7, lines 41-55), and wherein an area of the region of the first thickness is smaller than an area of the region of the second thickness (fig. 3 and col. 7, lines 41-55); and an island-like semiconductor layer (35, 62, 63) having a crystal structure over the region of the first thickness and the region of the second thickness, a gate insulating film 51 over an island-like layer; and a gate electrode 52 over the gate insulating film, wherein the island-like semiconductor layer entirely covers the region of the first thickness. Note that the first thickness is comprised of layers 33 and 34.

Re claim 13, the specification contains no disclosure of either the critical nature of the claimed arrangement or any unexpected results arising therefrom. Where patentability is said to be based upon particular chosen dimensions or upon another variable recited in a claim, the applicant must show that the chosen dimensions are critical. In re Woodruff, 919 F.2d 1575, 1578, 16 USPQ2d 1934, 1936 (Fed. Cir. 1990).

6. Claims 12 and 14, as understood, are rejected under 35 U.S.C. 102(e) as being anticipated by Adachi.

Adachi discloses in fig. 1 a semiconductor device comprising: a light-transmitting substrate 31; a base film 33 having a region of a first thickness and a region of a second thickness over one surface of the light- transmitting substrate, wherein the second thickness is smaller than the first thickness (fig. 3 and col. 7, lines 41-55), and wherein an area of the region of the first thickness is smaller than an area of the region of the second thickness (fig. 3 and col. 7, lines 41-55); a thin film transistor comprising a channel formation region, wherein at least a part of the channel formation region is provided over the region of the first thickness; source and drain regions (62, 63), wherein at least a part of source and drain regions is provided over the second thickness, wherein the channel formation region and the source and drain regions entirely cover the region of the first thickness -- Note that the first thickness is comprised of layers 33 and 34 -- a gate insulating film 51 over the channel formation region; and a gate electrode 52 over the gate insulating film.

Re claim 14, the specification contains no disclosure of either the critical nature of the claimed arrangement or any unexpected results arising therefrom. Where patentability is said to be based upon particular chosen dimensions or upon another variable recited in a claim, the applicant must show that the chosen dimensions are critical. In re Woodruff, 919 F.2d 1575, 1578, 16 USPQ2d 1934, 1936 (Fed. Cir. 1990).

Claim Rejections - 35 USC § 103

7. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

8. Claims 17 and 18 are rejected under 35 U.S.C. 103(a) as being unpatentable over Adachi.

Adachi discloses the device structure as recited in the claims including a metal oxide base film, but does not specifically disclose a silicon oxide base film or silicon nitride base film.

However, in a case such as this one, where an improvement is no more than "the simple substitution of one known element for another," *KSR Int'l Co. v. Teleflex Inc.*, 127 S.Ct. 1727, 1740, 82 USPQ2d 1385, 1396 (2007), no further analysis is required of the Examiner. See Ex parte SMITH, Appeal 2007-1925, (6/25/07) Slip Op. at 21. Also available at http://www.uspto.gov/web/offices/dcom/bpai/prec/fd071925.pdf).

9. Claims 19-22 are rejected under 35 U.S.C. 103(a) as being unpatentable over Adachi.

Adachi discloses the device structure as recited in the claims, but does not specifically disclose a semiconductor device being applied to an electronic instrument listed in the claim.

However, Examiner takes Official Notice that an electronic instrument selected from the group consisting of a personal computer, a video camera or a digital camera is conventional and well known. Therefore, it would have been obvious to one skilled in the art at the time the invention was made to have employed any of the various electronic instruments since Examiner takes Official Notice that due to their low power consumption, displays have become a necessary and indispensable structural element of an electronic instrument.

Conclusion

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Ahmed Sefer whose telephone number is (571)272-1921

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Sue Purvis can be reached on (571) 272-1236.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/A. Sefer/
Primary Examiner
Art Unit 2826